

## IN THE CLAIMS

What is claimed is:

- 1    **1.**    A memory controller connected to a semiconductor memory device, comprising:
  - 2                   a clock generating circuit that generates an output clock signal;
  - 3                   a data generating circuit that provides output digital data;
  - 4                   a predetermined number “m” data output terminals that provide output
  - 5                   data to the semiconductor memory device in parallel;
  - 6                   m output holding circuits for storing the output digital data
  - 7                   synchronously with the output clock signal;
  - 8                   a predetermined number “n” signal output terminals that provide
  - 9                   output strobe signals to the semiconductor memory device in synchronism
  - 10                  with the output data, where  $n < m$ ; and
  - 11                  a plurality of output delay circuits including one output delay circuit
  - 12                  for every “p” signal output terminal(s), where p is an integer greater than zero,
  - 13                  each output delay circuit delaying the output clock signal by a predetermined
  - 14                  amount to transmit an output strobe signal to the corresponding p signal
  - 15                  output terminal(s); wherein
  - 16                  each m output holding circuit is physically adjacent to a corresponding
  - 17                  one of the m data output terminals; and
  - 18                  the output of each output delay circuit is adjacent to the corresponding
  - 19                  p signal output terminal(s).

1    2.    The memory controller of claim 1, wherein:  
2                    the m output data output terminals and n signal output terminals are  
3                    linearly aligned with one another;  
4                    the m holding circuits are linearly aligned with one another; and  
5                    the plurality of output delay circuits are linearly aligned with one  
6                    another between m holding circuits and the aligned m data output terminals  
7                    and n signal output terminals.

1    3.    The memory controller of claim 1, wherein:  
2                    the value p is greater than one, and the value n is a multiple of p.

1    4.    The memory controller of claim 1, wherein:  
2                    value of p is selected from the group consisting of one and two.

1    5.    The memory controller of claim 1, wherein:  
2                    the value of p is one.

1    6.    The memory controller of claim 1, wherein:  
2                    the value of p is two; and  
3                    each of the plurality of output delay circuits has an output terminal  
4                    arranged equidistant from the corresponding two signal output terminals.

1    7.    The memory controller of claim 1, further including:

2                   a plurality of data input terminals that receive input data from the  
3 semiconductor memory device;

4                   a signal input terminal for every “q” data input terminals, where  
5 “q” is an integer greater than 2, each signal input terminal receiving an  
6 device input clock signal from the semiconductor memory device in  
7 synchronism with the input data;

8                   an input delay circuit corresponding to each signal input terminal  
9 that delays a received device input clock form the semiconductor memory  
10 device signal by a predetermined amount to generate an input strobe  
11 signal, the input delay circuits being arranged between the signal input  
12 terminals and positions where the input delay circuits output the input  
13 strobe signals; and

14                  an input holding circuit corresponding to each data input terminal,  
15 each group of q input holding circuits holding input data in synchronism  
16 with the input strobe signal from a corresponding input delay circuit;  
17 wherein

18                  the input data is transmitted to the data generating circuit through  
19 the data input terminals.

1    **8.**     The memory controller of claim 1, further including:

2                   a plurality of data input terminals that receive input data from the  
3 semiconductor memory device;

4                   a signal input terminal for every “q” data input terminals, where

5 “q” is an integer greater than 2, each signal input terminal receiving a  
6 device input clock signal from the semiconductor memory device in  
7 synchronism with the input data;

8 an input delay circuit corresponding to each signal input terminal  
9 that delays a received device input clock signal from the semiconductor  
10 memory device by a predetermined amount to generate an input strobe  
11 signal, the input delay circuits being arranged between the signal input  
12 terminals and positions where the input delay circuits output the input  
13 strobe signals; and

14 an input holding circuit corresponding to each data input terminal,  
15 each group of q input holding circuits holding input data in synchronism  
16 with the input strobe signal from a corresponding input delay circuit;

17 a first wiring corresponding to each data input terminal that  
18 transmits digital data to a corresponding input holding circuit; and

19 a second wiring corresponding to each input holding circuit that  
20 transmits the input strobe signal from a corresponding input delay circuit  
21 to the input holding circuit; wherein

22 the first and second wiring corresponding to each input holding circuit  
23 being essentially equal in length.

1 9. The memory controller of claim 1, wherein:

2 the m data output terminals are also data input terminals that receive  
3 input data from the semiconductor memory device in parallel; and

4                   the n signal output terminals are also signal input terminals for  
5                   receiving device input clock signals from the semiconductor memory device  
6                   in synchronism with the input data.

1   **10.**   The memory controller of claim 1, wherein:

2                   the output holding circuits transmit output digital data synchronously  
3                   with both a rising edge and a falling edge of the output clock signal.

1   **11.**   The memory controller of claim 1, further including:

2                   a plurality of data input terminals that receive input data from the  
3                   semiconductor memory device;

4                   a signal input terminal for every “q” data input terminals, where  
5                   “q” is an integer greater than 2, each signal input terminal receiving an  
6                   device input clock signal from the semiconductor memory device in  
7                   synchronism with the input data; and

8                   an input delay circuit corresponding to each signal input terminal  
9                   that delays a received device input clock from the semiconductor memory  
10                  device signal by a predetermined amount to generate an input strobe  
11                  signal, the input delay circuits being arranged between the signal input  
12                  terminals and positions where the input delay circuits output the input  
13                  strobe signals;

14                  an input holding circuit corresponding to each data input terminal,  
15                  each group of q input holding circuits holding input data in synchronism

16 with the input strobe signal from a corresponding input delay circuit;  
17 wherein  
18 the input holding circuits transmit input data to the data generating  
19 circuit synchronously with both a rising edge and a falling edge of the  
20 corresponding input strobe signal.

1 **12.** The memory controller of claim 1, further including:

2 the semiconductor memory device being coupled to the memory  
3 controller by the m data output terminals and the n signal output terminals.

1 **13.** The memory controller of claim 1, further including:

2 a circuit core region in which the clock generating circuit and data  
3 generating circuit are formed; and

4 an interface region surrounding the circuit core region in which the  
5 data output terminals, output holding circuits, signal output terminals, and  
6 output delay circuits are formed; wherein

7 each output holding circuit comprising a first latch circuit.

1 **14.** The memory controller of claim 13, further including:

2 the data output terminals are data input/output (I/O) terminals;

3 the signal output terminals are signal I/O terminals;

4 m input holding circuits corresponding to the data I/O terminals

5 formed in the interface region, each input holding circuit comprising a

6 second latch circuit connected to a corresponding data I/O terminal by a  
7 first wiring, the input holding circuits holding input data in synchronism  
8 with a corresponding input strobe signal; and  
9 an input delay circuit connected to each signal I/O terminal by a  
10 second wiring, each input delay circuit delaying a received device input  
11 clock from the semiconductor memory device signal by a predetermined  
12 amount to generate an input strobe signal, each input strobe signal being  
13 connected to a corresponding second latch circuit by a third wiring;  
14 wherein  
15 the length of the first wiring to each second latch circuit is essentially  
16 equal to the sum of the lengths of the second and third wirings corresponding  
17 to the same second latch circuit.

1 15. A memory controller connected to a semiconductor memory device, comprising:  
2 a predetermined number “m” data input terminals that receive  
3 input data from the semiconductor memory device;  
4 a predetermined number “n” signal input terminals, each signal  
5 input terminal receiving a device input clock signal from the  
6 semiconductor memory device in synchronism with the input data, where  
7  $m > n$ ;  
8 a data storing circuit for receiving digital data from the data input  
9 terminals;  
10 n input delay circuits that delay received device input clock signals

11 from the semiconductor memory device by a predetermined amount to  
12 generate input strobe signals;  
13 m input holding circuits that hold the input data in synchronism  
14 with the input strobe signals generated by the input delay circuits; and  
15 m data input wirings, each data input wiring transmitting an input  
16 data value from one data input terminal to a corresponding input holding  
17 circuit; and  
18 m signal input wirings transmitting one input strobe signal from  
19 one input delay circuit to a corresponding input holding circuit; wherein  
20 the data input wiring and signal input wiring for the same  
21 corresponding input holding circuit being essentially equal in length.

1 **16.** The memory controller of claim 15, wherein:

2 the input delay circuits are arranged between the signal input terminals  
3 and locations where the input delay circuits output the input strobe signals.

1 **17.** The memory controller of claim 15, wherein:

2 the input holding circuits transmit input data to the data generating  
3 circuit synchronously with both a rising edge and a falling edge of the  
4 corresponding input strobe signal.

1 **18.** The memory controller of claim 15, further including:

2 the semiconductor memory device being coupled to the memory



3 controller by the m data input terminals and the n signal input terminals.

1 **19.** The memory controller of claim 15, further including:

2 a circuit core region in which the data storing circuit are formed; and

3 an interface region surrounding the circuit core region in which the  
4 data input terminals, input holding circuits, signal input terminals, input delay  
5 circuits, signal input wirings, and data input wirings are formed; wherein

6 each input holding circuit comprising a first latch circuit.

1 **20.** The memory controller of claim 15, further including:

2 the m data input terminals and n signal input terminals are linearly  
3 aligned with one another; and

4 the m input holding circuits are linearly aligned with one another  
5 parallel to the data input terminals and signal input terminals.

1 **21.** The memory controller of claim 15, further including:

2 a clock generating circuit that generates an output clock signal;

3 a data generating circuit that provides output digital data;

4 a plurality of data output terminals that that provide output data to the  
5 semiconductor memory device in parallel;

6 a signal output terminal for every “q” data output terminals, where  
7 “q” is an integer greater than 2, each signal output terminal providing an  
8 output strobe signal to the semiconductor memory device in synchronism

9           with the output data;

10                 an output delay circuit for every “p” signal output terminal(s), where p

11           is an integer greater than zero, each output delay circuit delaying the output

12           clock signal by a predetermined amount to transmit an output strobe signal to

13           the corresponding p signal output terminal(s); and

14                 an output holding circuit corresponding to each data output terminal, each

15           group of q output holding circuits holding output data in synchronism with the

16           output strobe signal from the corresponding output delay circuit.